

PREPARE FOR THE NEXT GENERATION OF MEMORY: Is your application a good candidate?

Jackson Marusarz

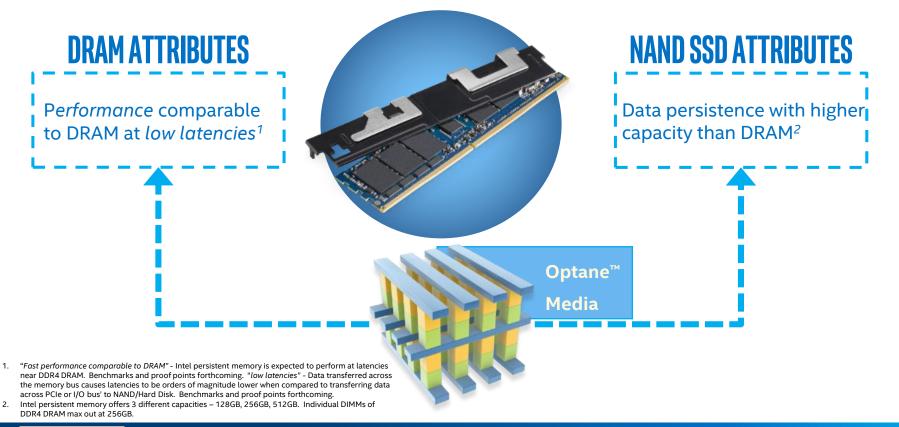
Senior Technical Consulting Engineer Compute Performance & Developer Products Division

Agenda

- Brief introduction to Intel[®] Optane[™] DC Persistent Memory
- Concepts and tools for enabling
 - Workload suitability analysis
 - Profiling and tuning workloads running with Intel Optane DC Persistent Memory
- Case Studies



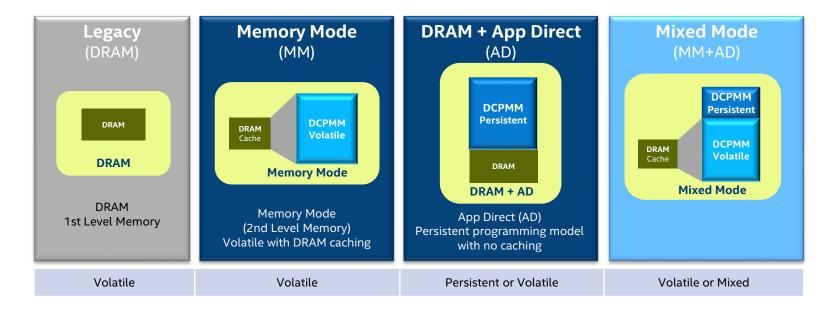
THE BEST OF BOTH WORLDS WITH INTEL® OPTANE™ DC PERSISTENT MEMORY



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PROGRAMMING MODELS





Will I benefit from Intel® Optane™ DC Persistent Memory?

- Do you need: Big Memory Fast Storage Memory Resilience?
- Are your workloads running out of DRAM memory?
- Is Disk I/O a large portion of your overhead?
- Does your warmup/data population phase takes a long time?

Use analysis tools to determine:

- How your system and applications may benefit from Intel[®] Optane[™] DC Persistent Memory
- The best and easiest ways to take advantage of Intel[®] Optane[™] DC Persistent Memory



Software Tools For Intel[®] Optane[™] DC Persistent Memory

Intel[®] VTune[™] Amplifier – Performance Analysis

- Platform Profiler find configuration issues and potential for larger memory
- Memory analysis design data structures for hot/warm/cool memory
- Memory analysis tune use of DCPMM memory
- Storage analysis are you CPU or I/O bound?

Intel[®] Inspector – Persistence Inspector

Finds missing/redundant cache flushes, PMDK logging errors, and more



Use cases for tools with Intel® Optane™ DC Persistent Memory

Before you have hardware (workload suitability)

- Transitioning from DRAM-only to Memory Mode
- Transitioning from DRAM-only to App Direct (non-persistent mode)
- Transitioning from DRAM-only to App Direct (persistent mode)

After you have hardware

• Tuning existing Intel[®] Optane[™] DC Persistent Memory usages



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Intel[®] VTune[™] Amplifier - Performance Profiler Analyze & Tune Application Performance & Scalability

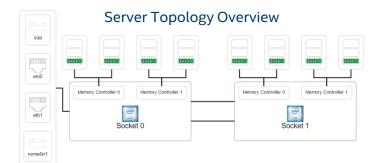
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Grouping: Function / Call Stack 🗸 🗐										
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▼ main\$omp\$parallel_for@269	7.915s 🛑	0s	0s	0s	0.055s	9				
▶ <kmp_invoke_microtask [op<="" p="" ←=""></kmp_invoke_microtask>	7.915s 🛑	0s	0s	0s	0.042s	8				
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Faster, Scalable Code, Faster

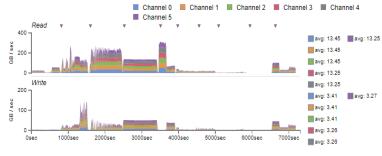
- Accurately profile C, C++, Fortran*, Python*, Go*, Java*, or any mix
- Optimize CPU/GPU, threading, memory, cache, MPI, storage & more
- Save time: rich analysis leads to insight
- Data displayed on the source code
- Easy set-up, no special compiles
- Cross-OS support and IDE integration



Intel[®] VTune[™] Amplifier - Platform Profiler



Traffic Patterns



Performance metrics on system topology

- Display current configuration
- Socket → Core → Internal Caches
- Socket → Memory Link → Memory Module
 Identify system configuration issues
- Inefficient memory module placements
- Need for faster storage
- Need for larger/faster memory
- Identify potential software issues
- Low CPU utilization
- NUMA-related issues (near vs. far memory accesses)
- Inefficient usage of memory/storage resources
 Compare different system configurations

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BEFORE YOU HAVE HARDWARE

- Transitioning from DRAM-only to Memory mode
- Transitioning from DRAM-only to AppDirect (non-persistent mode)
- Transitioning from DRAM-only to AppDirect (persistent mode)



DRAM-only -> Memory Mode (Big Memory - no code modification)

Look for applications with a memory footprint larger than DRAM but a hot working set size smaller than DRAM

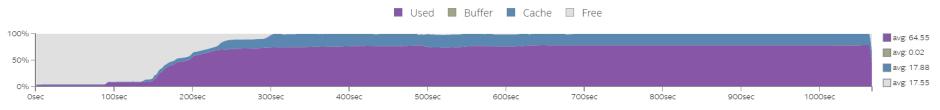
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du la							▶ matrix.c:126 (128 MB)		2,196,965,907	70,028,400,789	2,250,135	
Cors					_		[vmlinux]			117,903,537	65,701,971	0

Memory Access Analysis + Dynamic Memory Object Analysis

Memory Consumption Analysis

Memory Consumption with Platform Profiler

Memory Utilization



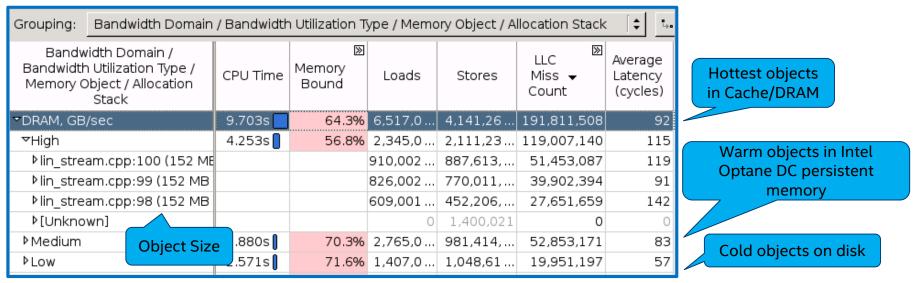
- Profile system wide
- Longer running workloads
- Correlate with other platform profiler metrics



DRAM-only ->App Direct (volatile) Mode (Big Memory - code modification required)

Identify objects to allocate in Intel[®] Optane[™] DC Persistent Memory:

- For objects larger than DRAM allocate in Intel® Optane™ DC Persistent Memory
- If an object is smaller than LLC allocate in Intel® Optane™ DC Persistent Memory because it will likely be cached



Memory Access Analysis + Dynamic Memory Object Analysis



Memory Access

DRAM-only ->App Direct (volatile) Mode (Big Memory - code modification required)

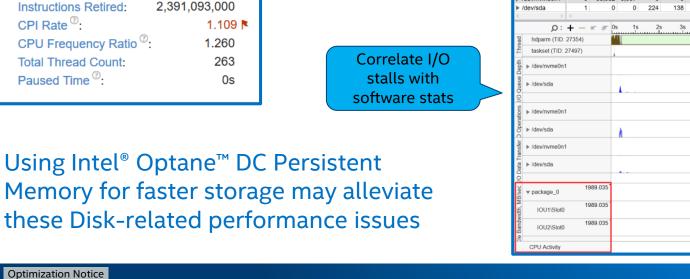
Intel[®] Optane[™] DC Persistent Memory reads are faster than writes:

- Put load heavy objects in Intel[®] Optane[™] DC Persistent Memory
- Put store heavy objects in DRAM

store neavy objects in Br	IC	dentify				
Grouping: Bandwidth Domain	/ Bandwidth) Utilization Ty	ype load/	store ratio	cation Stack	: [‡ <u></u> □
Bandwidth Domain / Bandwidth Utilization Type / Memory Object / Allocation Stack	CPU Time	⊠ Memory Bound	Loads	Stores	LLC Miss ✔ Count	Average Latency (cycles)
▼DRAM, GB/sec	9.703s 📒	64.3%	6,517,0	4,141,26	191,811,508	92
⊽High	4.253s	56.8%	2,345,0	2,111,23	119,007,140	115
♭lin_stream.cpp:100 (152 MB			910,002	887,613,	51,453,087	119
♭lin_stream.cpp:99 (152 MB			826,002	770,011,	39,902,394	91
▶lin_stream.cpp:98 (152 MB			609,001	452,206,	27,651,659	142
Þ[Unknown]			0	1,400,021	0	0
▶Medium	2.880s	70.3%	2,765,0	981,414,	52,853,171	83
ÞLow	2.571s	71.6%	1,407,0	1,048,61	19,951,197	57

Memory Access Analysis + Dynamic Memory Object Analysis

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2.113s

1.406s

Persistent Memory - code modification required

Identify disk related performance issues with Input and Output Analysis

Time wasted

waiting for disk

Disk Input and Output Disk Input and Output viewpoint (change)

Grouping: Storage Device / Partition

read by I/O Operation .

Good

Storage Device / Partition

/dev/nvme0n1

🗉 🖂 Collection Log \ominus Analysis Target 🙏 Analysis Type 🚯 Summary 📣 Bottom-up 📧 Platform

I/O Queue Depth V

write by I/O Operation

DRAM-only -> App Direct (non-volatile) Mode

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Elapsed Time ⁽²⁾: 6.571s

I/O Wait Time ^②:

CPU Time ⁽²⁾:



Summary Call Stack

3.000

2.000

1 000

Thread Running

Context Switches

I/O Wait

CPU Time I TIO APIs

✓ I/O Queue Depth V Queue Depth

Slow

Slow Good

Fast

Page Faults

I/O Operations Total

Operation Type ✓ ~flush

✓ mead

✓ write

I/O Data Transfer Total

Operation Type

Preemption

Synchronization

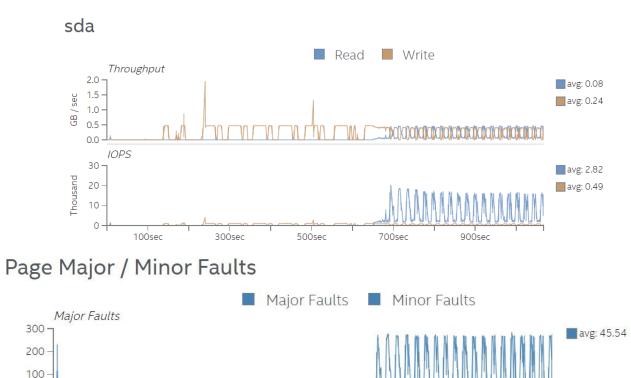
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2

I flush by I/O Operation

4s 5s

Disk Issues with Platform Profiler



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AFTER YOU HAVE HARDWARE

Tuning existing Intel[®] Optane[™] DC Persistent Memory usages

Tuning Intel[®] Optane[™] DC Persistent Memory Systems

Memory Access

Selapsed Time [™] : 22.976s		
CPU Time [®] :	22.612s	
	69.6% 🖻 of Pipeline	Slots
L1 Bound [®] :	12.5% 🖻 of Clocktick	(S
L2 Bound [®] :	0.4% of Clocktick	(S
L3 Bound [®] :	2.9% of Clocktick	(S
③ DRAM Bound ^② :	0.0% 🖻 of Clocktic	Bound by Intel [®] Optane [™] DC
	49.0% of Clocktic	
Persistent Memory Bandwidth Bound ⁽²⁾ :	0.0% of Elapsed	
Local Persistent Memory $^{\odot}$:	100.0% of Clocktick	(S
Remote Persistent Memory ^② :	0.0% of Clocktick	(S
Loads:	10,519,515,576	
Stores:	4,292,228,763	
③ LLC Miss Count ^② :	36,902,214	
Average Latency (cycles) ^② :	41	
Total Thread Count:	16	
Paused Time [®] :	, Os	
*N/A is applied to metrics with undefined value. There is no a	lata to calculate the metric.	

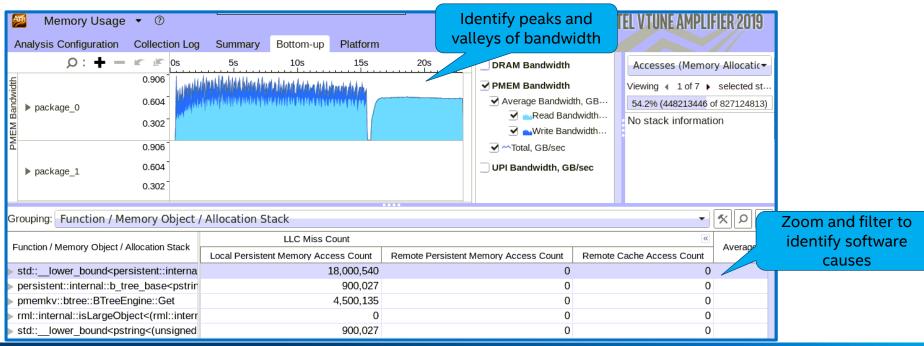
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Memory Access

Tuning Intel[®] Optane[™] DC Persistent Memory Systems Intel[®] VTune[™] Amplifier (Cont'd)

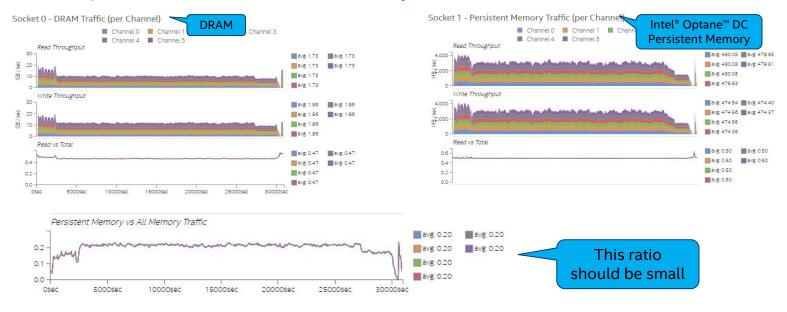
- View Intel[®] Optane[™] DC Persistent Memory bandwidth over time
- Correlate data with CPU metrics and source code information



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Tuning Intel[®] Optane[™] DC Persistent Memory Systems VTune[™] Platform Profiler

For Memory mode systems – make sure DRAM Bandwidth is much higher than Intel[®] Optane[™] DC Persistent Memory Bandwidth



Optimization Notice



Find Missing/Extra Flushes/Commits

Intel[®] Inspector - Persistence Inspector

Target User

 Persistent memory programmers

Problem	15								ę	
ID 🔺	۲	Туре		Sources		Module	s	State		
⊞ P1	8	Missing cache flu	sh	MSVCR120D.dll:0	x4B	MSVCR1	20D.dll	P Ne	w	
± P2	8	Missing cache flu	sh	trace.pmem.cpp:	201	tachyon	.exe	R Ne	w	
± P3	Δ	Missing cache flu	sh before unmap()	pmem_windows.	срр	tachyon	.exe	Pe Ne	w	
Descripti	on 🔺		Source	Function	Mo	dule	Variabl	e	^	
Controlled variable trace.pmem.cpp:243 do_render tachyon.exe								1		
241		color	t *pixel = srb[width * y + >	1;	tachyon	.exe!	lo_re		
242		*pixel	<pre>*pixel = render_one_pixel(x, y, local tachyon.exe!threa</pre>							
243	243 rs->pixels_stored++; tachyon.exe!trace							crace		
244		drawing.put_pixel(*pixel); tachyon.exe!trace								
245		}				tachyon	.exe!	cende		
Unflus	hed m	emory store	trace.pmem.cpp	:242 do_render	tack	iyon.exe				
240		{				tachyon	.exe!	io re		
241		color	t *pixel = &rb[width * y + >	1;	tachyon	.exe!1	threa		
242		*pixel	= render one p	ixel(x, y, lo	cal	tachyon	.exe!1	race		
243		rs->pi	xels_stored++;			tachyon	.exe!t	crace		
244		drawin	g.put pixel(*pi			tachyon	ovela	anda		

What does it do?

- Finds persistent memory programming errors
- Detects:
 - Missing / redundant cache flushes
 - Missing store fences
 - Out-of-order persistent memory stores
 - PMDK transaction redo logging errors
- As a design tool, it finds places to insert flushes
- As a performance tool, it finds redundant flushes

How to Use Intel[®] Inspector - Persistence Inspector

Note: PMDK = Persistent Memory Developer Kit (formerly NVML)

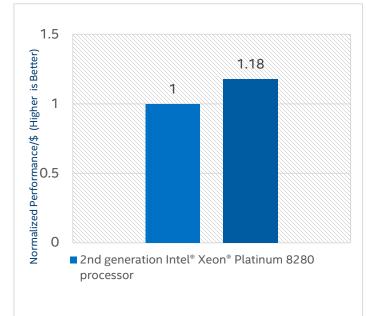




CASE STUDIES



http://www.sas.com



SAS (VIYA 3.4)*



XEON

APPLICATION

SAS* is a world leader in analytics and Artificial Intelligence. SAS Viya* provides a unified, open analytics platform replete with cutting-edge algorithms and AI capabilities. SAS Viya is a cloud- enabled, in-memory analytics engine that provides quick, accurate, and reliable analytical insights.

CUSTOMER CHALLENGES

• Customers are currently limited by memory capacity, which restricts the volume of datasets that can be stored close to the CPU, thereby limiting the potential to improve query response times. Expanding the memory footprint to overcome this challenge is often cost-prohibitive for customers.

SOLUTION

- With 2nd generation Intel® Xeon® Scalable processors and Intel® Optane[™] DC persistent memory (Memory Mode), SAS can take advantage of larger available memory capacity per system, while making it a more cost-effective solution for customers.
- Customers can now keep multiple large datasets used for gradient boosting models in memory, with **little to no performance degradation**, and **at a reduced cost** (see chart showing up to 18% performance improvement for a given cost)¹.

VALUE PROPOSITION

• Better performance at similar cost - SAS customers can benefit from improved analytics response times, with better TCO¹, and while meeting performance expectations.

Performance Metric: Completion Time for 3 Concurrent Logistics Regression Tasks (400GB Datasets), Per \$TCO (i.e., Perf/\$TCO)²

1 - Performance results are based on testing by Intel and SAS on 02/15/19 and may not reflect all publicly available security updates. No product or component can be absolutely secure. For complete testing configuration details, see <u>Configuration Section</u>. 2 - Pricing Guidance as of March 31, 2019 & valid until Jun 29, 2019. Intel does not guarantee any costs or cost reduction. You should consult other information and performance tests to assist you in your purchase decision.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance.



Configuration Details

SAS[®] Viya[®]*; In-memory Analytics: SAS[®] Viya 3.4 VDMML application. Workload: 3 concurrent logistic regression tasks each running on 400GB datasets. Testing by Intel and SAS completed on February 15, 2019. Pricing Guidance as of March 31, 2019 & valid until Jun 29, 2019. Intel does not guarantee any costs or cost reduction. You should consult other information and performance tests to assist you in your purchase decision.

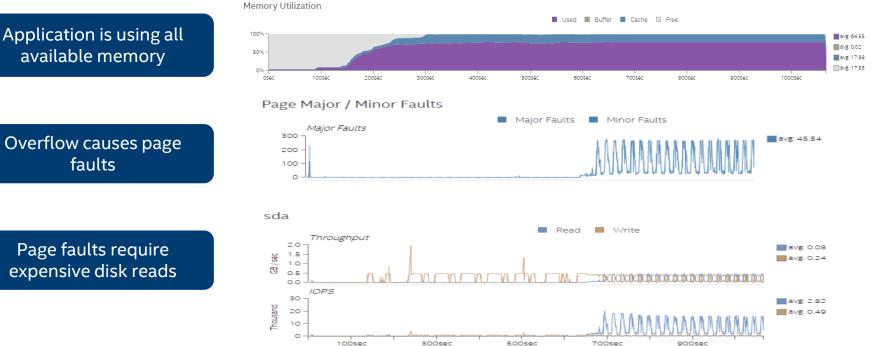
BASELINE: 2S Intel® Xeon® Platinum 8280 processor, 2.7GHz, 28 cores, turbo and HT on, BIOS SE5C620.86B.0D.01.0286.011120190816, 1536GB total memory, 24 slots / 64GB / 2666 MT/s / DDR4 LRDIMM, 1x 800GB, Intel SSD DC S3710 OS Drive + 1x 1.5TB Intel Optane SSD DC P4800X NVMe Drive for CAS_DISK_CACHE + 1x 1.5TB Intel SSD DC P4610 NVMe Drive for application data, CentOS Linux* 7.6 kernel 4.19.8.

NEW: 2S Intel® Xeon® Platinum 8280 processor, 2.7GHz, 28 cores, turbo and HT on, BIOS SE5C620.86B.0D.01.0286.011120190816, 1536GB Intel Optane DC persistent memory configured in Memory Mode(8:1), 12 slots / 128GB / 2666 MT/s, 192GB DRAM, 12 slots / 16GB / 2666 MT/s DDR4 LRDIMM, 1x 800GB, Intel SSD DC S3710 OS Drive + 1x 1.5TB Intel Optane SSD DC P4800X NVMe Drive for CAS_DISK_CACHE + 1x 1.5TB Intel SSD DC P4610 NVMe Drive for application data, CentOS Linux* 7.6 kernel 4.19.8.



GraphX Workload Analysis

Runs with large datasets are failing



Overflow causes page faults

available memory

Page faults require expensive disk reads

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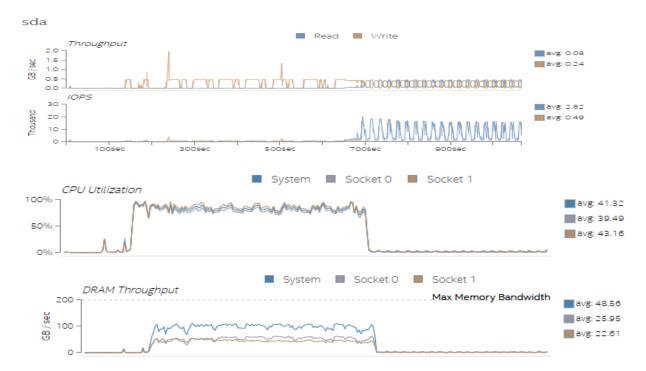
GraphX Workload Analysis

Runs with large scale factor are failing

Page faults and disk IO correlate on timeline

CPU Utilization drops

DRAM Throughput drops



Optimization Notice

Graph V Markeland Analysis

Runs

Pag

cor

Conclusion:

- Application is using all available memory and showing high disk and paging activity.
- The application is not bound by the memory bandwidth or CPU saturation. This is an indicator that application is bound by the capacity of the memory.
 - Adding Intel[®] Optane[™] DC Persistent Memory in Memory Mode allowed GraphX to scale to these larger datasets.

avg: 41.32 avg: 39.49 avg: 43.16

0.08 0.24

2.82 0.49

System Socket 0 Socket 1

It's not just a raw performance calculation - it's TCO, performance, and scalability



Summary

- Intel[®] VTune[™] Amplifier brings its best-in-class performance profiling and tuning to Intel[®] Optane[™] DC Persistent Memory systems
- Including use cases:

Before you have hardware

- Transitioning from DRAM-only to Memory mode
- Transitioning from DRAM-only to AppDirect (non-persistent mode)
- Transitioning from DRAM-only to AppDirect (persistent mode)
 After you have hardware
- Tuning existing Intel[®] Optane[™] DC Persistent Memory usages





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